ANNA UNIVERSITY OF TECHNOLOGY, COIMBATORE

B.E. / B.TECH DEGREE EXAMINATIONS: NOV / DEC 2010

REGULATIONS: 2008

THIRD SEMESTER: ECE

080290010 - DIGITAL ELECTRONICS

TIME: 3 Hours **Max. Marks: 100**

PART-A

(20 x 2 = 40 Marks)

ANSWER ALL QUESTIONS

1. Prove that A+A'B= A+ B
2. Minimize F = *L* (0, 1, 3, 4, 5) using K-map
3. Draw a tristate inverter and draw its truth table.
4. A certain logic family specifies that the highest logical 0 output of a gate 2.0v. The gate input will be interpreted as a 0 for any voltage below 2.8v.In addition, a 3v spike applied to the gate input will appear on the output of the gate as a 3v spike. What is the noise immunity and the noise margin of this family?
5. Represent a half adder in block diagram form and also its logic implementation.
6. Implement the following function using suitable multiplexer

   F(x, y, z) = Im (0, 2, 5, 7)
7. What are the applications of decoders?
8. Give the seven segment code to display "A" in a common anode LED.
9. Draw the circuit of T flip flop using SR flip flop.
10. Give the excitation table of JK flip flop.
11. What do you mean by parallel and serial counters?
12. Define shift registers. What are its types?
13. What are the differences between static and dynamic RAM?
14. List the different types of ROM.

15. Draw the circuit of a MOSFET RAM cell.

16. Write short notes on PAL

17. Distinguish between synchronous sequential circuits and asynchronous sequential circuits.

18. Differentiate a Moore machine and Mealy machine.

19. What is fundamental mode?

20. Define critical race.

PART – B

(5 X 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. Simplify using Quine Mcklusky method and verify using K-map

F (A,B,C,D) = L m(3,4,5,7,9, 13, 14, 15) (12)

22 (a).Implement F = *(AB+AB)(C+D)* using NOR gates. (4)

(b). Draw a TTL gate that gives an output (AB)' and explain its operation. (8)

23. Design a BCD to excess 3 code converter using four full adders. (12)

24. Design a 3 bit binary counter using T flip flop that has a repeated sequences of six states. 000-001-010-100-101-110. Give the state table, state diagram and logic diagram. (12)

25. Draw the five bit Johnson counter and explain the operation. (12)

26. Explain the basic structure of a 256 x 4 static RAM with neat diagram. (12)

27. A combinational circuit is defined by functions

F1(A, B,C) = I(Q, 1,6,7)

F2(A,B,C) = I(2,3,5,7).

Implement the circuit with a PLA having three inputs, three product terms and two Outputs. (12)

28. What is a Hazard? Discuss in detail how hazards can be eliminated. (12)

**********THE END**********